UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,905	06/25/2003	Rafael Kedem	03-0177	4902

24319 7590 03/20/2007
LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
DOAN, NGHIA M	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

B/

Office Action Summary	Application No.	Applicant(s)	
	10/603,905	KEDEM, RAFAEL	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/25/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to the Application 10/603,905 filed on 06/25/2003. Claims 1-17 are pending.

Information Disclosure Statement

2. The Information Disclosure Statement filed on 06/25/2003 is acknowledged.

Claim Objections

3. Claims 1 and 6 are objected to because of the following informalities:

As per claim 1, line 11, replaces "IP block" with "pre-diffused IP block".

As per claim 6, line 12, replaces "IP block" with "pre-diffused IP block".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Butts et al., (Butts) (US Patent 6,539,535) (whole document).

6. With respect to claims 1, 6, 11, and 15, Butts discloses a method/apparatus for exposing pre-diffused IP blocks (fig. 22, LEs[526]) in a semiconductor device (fig. 1B)

for prototyping based on hardware emulation (whole document, particular as Abstract, col. 1, ll. 18-22, col. 3, ll. 117-34 and col. 4, ll. 8-14), comprising:

(claim 6) a multiplexer (whole document, particular as fig. 22, Mux [802]);

(claims 1, 6, and 11) connecting interface pins (whole document, particular as fig. 22, tri-state [446]) of at least two pre-diffused IP blocks (whole document, particular as fig. 22, LE[526] and fig. 2 as LO BLOCK) in a semiconductor device (whole document, particular as fig. 1B, LO BLOCK) to input ports of a multiplexer (whole document, particular as fig. 22, see blocks[800]);

(claims 1, 6, and 11) connecting an output port of said multiplexer (whole document, particular as fig. 22, Probe data streams [808]) to an I/O pin of said semiconductor device (whole document, particular as fig. 1, fig. 2, I/O [436]);

(claims 1, 6, and 11) providing an address to said multiplexer through a configuration pin (whole document, particular as fig. 22, configuration pin (Probe Sequence Memory [806]) of said semiconductor device to decide which of said interface pins is actually connected to said I/O pin (whole document, particular as fig. 1, control pin and fig. 22, Probe Sequence Memory [806], col. 15, ll. 23-55); and

(claims 1, 6, and 15) connecting said I/O pin to a reusable field programmable device (Field Programmable Pate Array (FPGA)) so that an IP block having said interface pin is selected for prototyping (whole document, particular as fig. 11 and fig. 22, col. 1, ll. 25-35, col. 2, ll. 32-47, col. 13, ll. 19-29, and col. 15, ll. 57-66).

7. With respect to claims 2, 7, and 13, Butts discloses wherein said multiplexer has two input ports (whole document, particular as fig. 22, Mux[802] has 1-144).

8. With respect to claims 3, 8, and 14, Butts discloses wherein said multiplexer has at least three input ports (whole document, particular as fig. 22, Mux[802] has 1-144).

9. With respect to claims 4, 9, and 16, Butts discloses wherein said reusable field programmable device is a field programmable gate array (whole document, particular as fig. 11 and fig. 22, col. 1, ll. 25-35, col. 2, ll. 32-47, col. 13, ll. 19-29, and col. 15, ll. 57-66).

10. With respect to claims 5, 10, and 17, Butts discloses wherein said reusable field programmable device is a programmable logic device (whole document, particular as PLD including PLAs and PALs, or FPGA) (fig. 11 and fig. 22, col. 1, ll. 25-35, col. 2, ll. 32-47, col. 13, ll. 19-29, and col. 15, ll. 57-66).

11. With respect to claim 12, Butts discloses wherein said semiconductor device is based on a slice (whole document, particular as fig. 1 and fig. 23).

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nghia M. Doan
Patent Examiner
AU 2825
NMD

3/16/07
THUAN V. DO
PRIMARY PATENT EXAMINER